CLEAN VERSION OF THE AMENDMENTS

IN THE SPECIFICATION

Paragraph beginning at page 6, line 21:

Before the LOCOS isolation process is performed within the second area, the first area, designated for the STI process, and an active region within the second area are masked, at the step 302. Using this mask step, the first area designated for the STI process is protected from the LOCOS isolation process. Next at the step 304, the layer of nitride is etched from the surface of the substrate in areas not protected by the mask deposited in the step 302. At the step 306, the mask covering the nitride within the second area and the mask covering the first area, are removed. At the step 308, the LOCOS isolation process is performed, forming a layer of field oxide in the substrate, separated by thin oxide regions, as described above. At the step 310, the second area designated for the LOCOS isolation process and the active regions within the first area, is masked. The second area designated for the LOCOS isolation process is protected from the STI process by this mask. Next, at the step 312, the unmasked areas within the first area, designated for the STI process, are etched to remove the layers of oxide and nitride and a shallow trench is formed within the substrate. Next, at the step 314, the mask over both the second area, designated for the LOCOS isolation process, and the active region within the first area, is then removed. At the step 316, the trenches formed within the substrate are filled. At the step 318, after both the LOCOS isolation process has been performed over the second area and the STI process has been performed over the first area, at least one SRAM cell is implemented in the first area and at least one flash EPROM cell is implemented in the second area, in any appropriate manner known to those skilled in the art. Note that several steps which are known to those skilled in the art, such as channel stop implants, etc., have not been described herein, in order to highlight the major process steps within the method of the present invention and the differences between the present invention and the prior art.

IN THE CLAIMS:

1. (Amended) A semiconductor device comprising:

a common substrate;

an SRAM device implemented on the common substrate and isolated by a first isolation technique; and

a flash EPROM device implemented on the common substrate and isolated by a second isolation technique,